MEDIA ALERT

SmartDV™

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SmartDV to Exhibit at Virtual Samsung SAFE Forum 2020 with Portfolio of Design and Verification IP

Attendees Can Learn How SmartDV Design and Verification Solutions Enable Users to Get to Market Quickly, Confidently

SAN JOSE, CALIF — October 20, 2020 —

WHO: SmartDV™ Technologies, the ***Proven*** and ***Trusted*** choice for Design and Verification Intellectual Property (IP)

WHAT: Will highlight its Design and Verification IP portfolio at Samsung's SAFE™ Forum 2020, along with SmartConf testbench generator, an add-on automation tool to its Verification IP portfolio, and Smart ViPDebug™, a visual protocol debugger that reduces debug time. Specific Design and Verification IP to be showcased includes:

- Verification IP for Arm® AMBA® CHI, CXS and LPI protocols
- Memory controller Design IP for high-speed HBM2/2E, HBM3, GDDR6 and LPDDR4/5 memories
- Design IP for video, imaging and entertainment systems such as V-by-One, VESA DSC, HDCP 2.3, HDMI CEC, HDMI eARC, CXP and SLVS-EC.
- Design IP for PCIe® CXL its new Verification IP that supports MIPI A-PHY v1.0, the industry-standard, long-reach serializer-deserializer (SerDes) physical layer interface.

SmartDV will also present its RISC CPU Verification tool and provide on-demand demonstrations of its Smart ViPDebug™, a visual protocol debugger that reduces debug time.

WHEN: Wednesday, October 28, beginning at 10 a.m. P.D.T.

WHERE: Online**.** Register at the Samsung SAFE Forum 2020 website.

Attendees can schedule virtual or meetings to learn more about SmartDV's Design and Verification IP solutions and how they enable users to get to market quickly and confidently at demo@smart-dv.com.

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Design and Verification IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. SmartDV offers high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification and RISC-V CPU verification. All of its Design and Verification IP solutions can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

Connect with SmartDV at:
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